A 0.13 μm High-Performance SOI Logic Technology with Embedded DRAM for System-On-A-Chip Application

H.L. Ho, M.D. Steigerwalt, B.L. Walsh, T.L. Doney, D. Wildrick, P.A. McFarland, J. Benedict, K.A. Bard, D. Pendleton, J.D. Lee, S.L. Maurer, B. Corrow, D.K. Sadana

IBM Microelectronics Semiconductor Research and Development Center (SRDC)
2070 RT 52, Hopewell Junction, NY 12533 USA

Abstract

In this paper, we report the successful implementation of a 0.13 μm high-performance Silicon-On-Insulator (SOI) logic technology to produce a 0.13 μm logic-based embedded DRAM (eDRAM) on substrates composed of both bulk Si and SOI or *Pattern SOI*. eDRAM macros are constructed in bulk regions of the wafer and high-performance logic circuits lie on SOI. Pattern SOI wafers are produced by blocking out selected regions of p-type Si wafers from the Separation by Implantation of Oxygen (SIMOX) implant using a thick (> 1μm) hard mask. Test results indicate that SOI eDRAM yield and retention characteristics are comparable to bulk eDRAM. Based on ring oscillator tests, the use of 0.13 μm SOI logic devices improves switching speeds by > 20% over 0.13 μm bulk technology at 1.2 Vdd. These results pave the way for future generations of low power SOI System–On–A-Chip (SOC) Applications, starting at the 0.1 μm node.

Introduction

Two major concerns that confront microprocessor technologies at the 0.13 μm node and beyond are – (1) power consumption and (2) die size. The former can be scaled by lower power supply voltages (Vdd) and by use of SOI wafers. By utilizing SOI as the substrates, lower junction capacitance can be realized [1]. The latter can be scaled by replacing SRAM blocks with embedded DRAM (eDRAM) blocks. Although not as fast as SRAM, the eDRAM cell size is considerably smaller than an SRAM cell, as much as 8X smaller than an SRAM cell, when designed at the same lithographic dimensions. The combination of trench-based eDRAM with high-performance logic on bulk silicon wafers has been successfully demonstrated [2]. However, integration of eDRAM with high-performance logic on SOI substrates becomes more of a challenge. If one builds eDRAM arrays in or on SOI wafers, the pass transistor for each cell will be subjected to floating body effects [3]. This situation will cause unacceptably high and variable leakage of the array pass transistor.

This paper describes the process methodology and initial results of utilizing high-performance 0.13 μm SOI logic technology to produce high-performance eDRAM on *Pattern SOI wafers* for SOC applications. In a Pattern SOI wafer, the majority of the wafer is SOI with "islands" of bulk silicon embedded within the wafer. Trench–based eDRAM macros are built in the bulk (p-type) silicon islands while high-performance logic circuits are built on SOI - this circumvents any floating body problems for the array pass gate if the eDRAM were to be built on SOI. eDRAM on Pattern SOI has been reported previously [4], however, in that work very large bulk areas were created (> 2 cm). In this work, the bulk areas provided are much smaller in scale (~ 100 μm). One of the key issues facing eDRAM on Pattern SOI is whether it is possible to create defect-free bulk regions such that a cell's retention time is not negatively impacted by crystal defects. Test macros of eDRAM have been processed and initial electrical results indicate that yield and retention characteristics of SOI eDRAM are comparable to those built on conventional bulk Si wafers. Logic performance – as reflected in ring oscillator tests – indicate a 40% boost in speed over their bulk counterparts at Vdd of 1.2 V.

Pattern SOI Fabrication

The process to form pattern SOI wafers is shown in a schematic in Fig. 1(a) – 1(d). After deposition of 1.2 μm BSG and 180 nm of nitride (Fig. 1(a)), a lithographic process of defining the bulk regions is carried out and the hard mask is reactive ion etched (RIE) down to the silicon surface. After the hard mask has been patterned (Fig. 1(b)), an 80 nm nitride film is deposited and etched to the Si surface to form sidewall spacers. After the SIMOX implant process (Fig. 1(c) the hard mask is stripped and the wafer is annealed at temperatures of ~ 1300°C in an argon-oxygen ambient (Fig. 1(d)). Figure 1(e) is a scanning electron microscope (SEM) image that shows the SOI/bulk silicon border and clearly defined SOI and bulk field regions. Moreover, the difference in step height between bulk and SOI is minimal - on the order of 10 – 20 nm.
Test macros of eDRAM have been processed and characterized using two different Pattern SOI masks. The first pattern mask – which we denote as *SC1* - blocks out

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an entire eDRAM macro from the oxygen implant (i.e. array, support, and peripheral circuits lie in bulk). The second pattern mask – which we denote as *SC2* - blocks ONLY the eDRAM array capacitors and eDRAM array well from the SIMOX implant (i.e. only peripherals and support circuitry of the eDRAM macro lie on SOI). Both pattern masks are shown schematically in Fig. 2.

Typical crystal defects that are formed at the SOI/bulk border are shown in Fig. 3(a). These defects include – (a) localized thin stacking faults (< 0.25 μm in width), (b) small dislocation loops. Stacking fault formation results from shifts in the {111} Si stacking sequence at the border between SOI and bulk Si during the SIMOX anneal; the presence of small dislocation loops is the result of implantation knock-on of the hard mask material into SOI. The defects themselves are restricted to a depth no greater than thickness of the SOI and are not observed to propagate into the bulk region. Failure analysis of eDRAM macros after the STI process module reveals that *any* defects produced by the Pattern SIMOX process do not come into play as they are completely removed via the shallow trench isolation (STI) etch process (see Fig. 3(b)).

SOI eDRAM Process Methodology

The process methodology of fabricating eDRAM in Pattern SOI is similar to fabricating eDRAM in bulk [2]. eDRAM trench capacitors are produced soon after Pattern SOI wafer formation. Due to stringent leakage requirements for an eDRAM cell, array devices are created using specific eDRAM masks to define its own retrograde well and (lightly-doped) extension process. Array, as well as I/O devices, are created using a thick gate oxide (5.2 nm); eDRAM support circuitry are created with thin gate oxides (2.2 nm). A clear distinction between bulk eDRAM and Pattern SOI eDRAM, however, is in the construction of the support and peripheral devices. For Pattern SOI, eDRAM's logic circuits are constructed using 0.13 μm SOI technology ("9S"). The process sequence to manufacture eDRAM in Pattern SOI is shown in block diagram form in Fig. 4. It can be shown that fabricating eDRAM in SOI requires only two additional masks over the eDRAM bulk case ("8SF") – (a) the patterning of the SOI wafers, (b) an eDRAM Nwell mask to contact the trench capacitors (i.e. plate). An SEM micrograph of eDRAM (lying in bulk) and SOI logic is shown in Fig. 5.

Electrical Results

Our findings suggest that yield and retention behavior of eDRAM arrays in Pattern SOI is similar to those created in bulk silicon and that the Pattern SOI process does not create any additional leakage in an eDRAM array. Fig. 6 is a chart that shows retention time plots (normalized log distribution of bit fails as function of retention) of array diagnostic monitors (ADMs) produced on - (a) bulk using the industry-standard 8SF-0.13 μm process, (b) SC1 using the 9S-0.13 μm SOI process, (c) SC2 using the 9S-0.13 μm process. (The ADM is a macro that specifically tests eDRAM cell functionality in an array environment – here, 524K bits – and its retention characteristics). The chart shows that first retention fails of eDRAM bits in either Pattern SOI mask occur at 128 ms. Early retention fails for bulk eDRAM occur between 128 and 256 ms. The slightly higher single cell failcount at lower retention times is largely due to the smaller devices present in the high-performance SOI process technology and which contribute to higher off-state leakage of the array device (Ldrawn = 0.22 μm). The magnitudes of other leakage paths within a cell – e.g. node junction leakage, node dielectric leakage – are similar between SOI eDRAM and bulk eDRAM. Figure 7 is a wafer bitfail map of ADMs representative of our Pattern SOI hardware using the SC2 mask and the 0.13 μm SOI logic front-end process. Thus, all support and peripheral circuits – designed to work specifically with bulk Si processing – were processed using the 0.13 μm SOI technology. The wafer map – taken at ~ 9 ms retention – shows that the majority of the 524 K ADMs are "screen-perfect" – i.e. all bits are fully-functional.

The advantages of using SOI-based logic technology are clearly evident in the increased drive currents, which, in turn, lead to increased device performance. Fig. 8 is a plot of PFET and NFET drive currents of the bulk 0.13 μm logic technology and 0.13 μm SOI logic technology; drive currents of SOI devices are ~40% greater than bulk at 1.2 Vdd. The SOI process technology results in significantly lower ring oscillator delays of the SOI devices over bulk devices. Fig. 9 is a plot of the stage delay of SOI and bulk devices as a function of Vdd measured on a 3-way NAND (65 stage, 0.12 μm channels, Fan Out = 3). The delays on SOI rings are reduced ~ 40% compared to bulk rings at 1.2 Vdd and ~35% at 0.9 Vdd. Part of the increase in device and ring performance is because of the shorter channel lengths in the SOI technology compared to bulk technology.

Conclusions

0.13 μm logic-based eDRAM macros have been successfully fabricated in Pattern SOI wafers using a 0.13 μm high-performance SOI logic process. The Pattern SOI process – which forms both bulk and SOI regions on the same wafer – allows eDRAM macros to be built in bulk Si while logic circuits are built on SOI. Our findings indicate SOI eDRAM yield and retention are similar to eDRAM produced on bulk Si. Logic circuit performance is improved by ~ 35 – 40% over those created in bulk because of the use of SOI process technology at power supply voltages of 1.2 Vdd or less. These encouraging results allow one to easily integrate dense, high-performance eDRAM in future SOI circuit designs.

References

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3. I K Kwon et al., IEDM Tech. Dig., p. 605 (1996).
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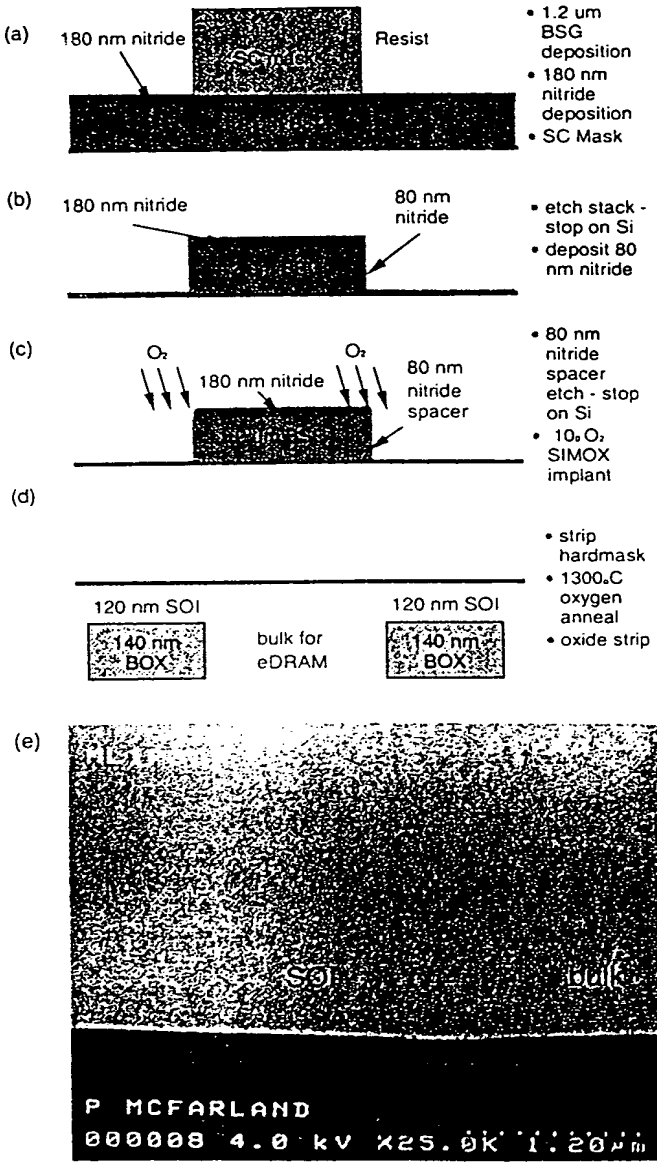

Figure 1: Process to form Pattern SOI wafers -
- (a) Hard mask film deposition and lithography
- (b) Hard mask stack etch, 80 nm nitride spacer deposition
- (c) Nitride spacer etch, 10" SIMOX implant
- (d) 1300°C SIMOX anneal and oxide strip
- (e) SEM of Pattern SOI wafer showing the border between SOI and bulk

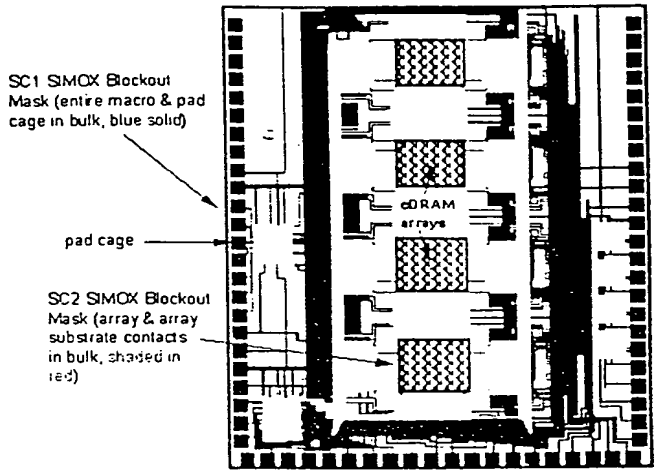

Figure 2: Schematic of ADM macro and eDRAM Substrate Contact (SCx) masks used to create bulk regions for eDRAM in Pattern SOI. SC1 (solid blue line) is used to block out entire eDRAM macro from SIMOX; SC2 (shaded red) is used to block the eDRAM array and array well from SIMOX.

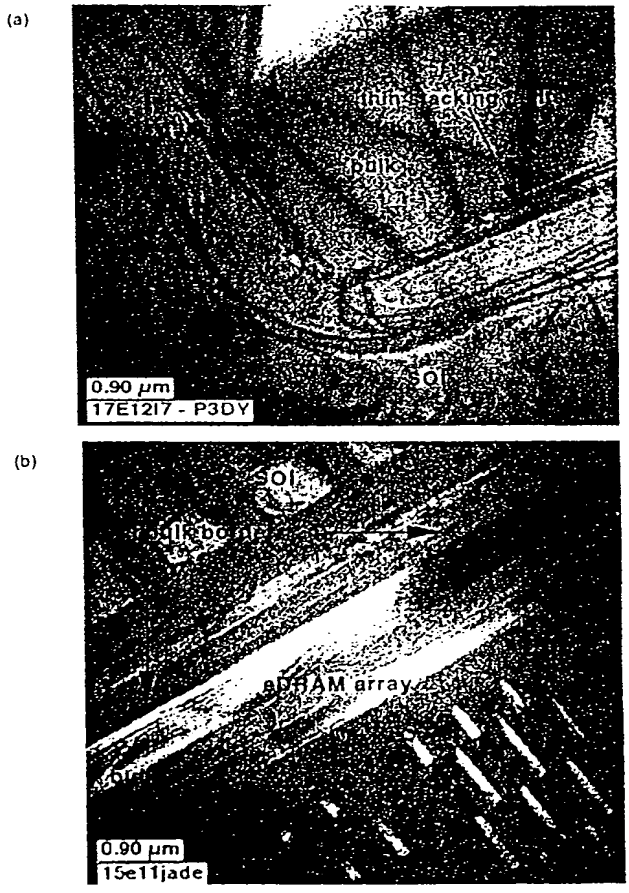

Figure 3 : Plan-view Transmission Electron Micrographs (TEM) of Pattern SOI wafers – (a) after SIMOX anneal, (b) after STI planarization. Crystal defects in substrate are removed via STI etch.

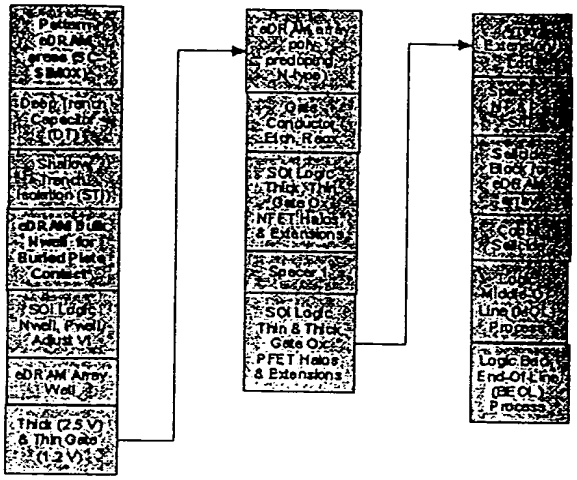

Figure 4: Block Diagram of eDRAM process on Pattern SOI using the SC2 SIMOX blockout mask; additional masks necessary for SOI eDRAM – beyond bulk eDRAM - are denoted in bold typeface.

Figure 5: SEM of SOI/bulk border of an SC2-patterned eDRAM macro – bulk region with trench capacitor on right, SOI region with silicided diffusions on left. Cu wire runs across bulk and SOI.

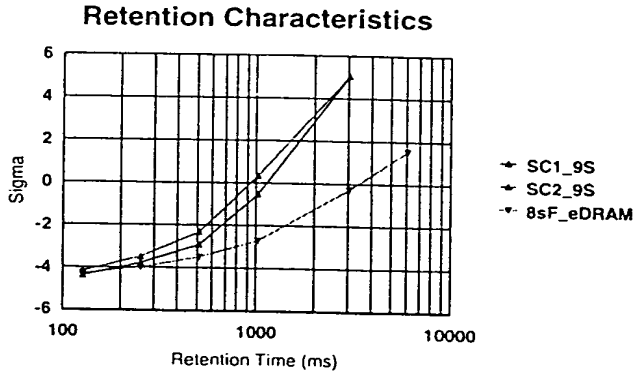

Figure 6: Normalized log distribution of bit fails as function of retention on Array Diagnostic Monitors (ADMs) produced in – (a) bulk (8SF), (b) SC1 using 0.13 µm 9S SOI, (c) SC2 using 0.13 µm 9S SOI.

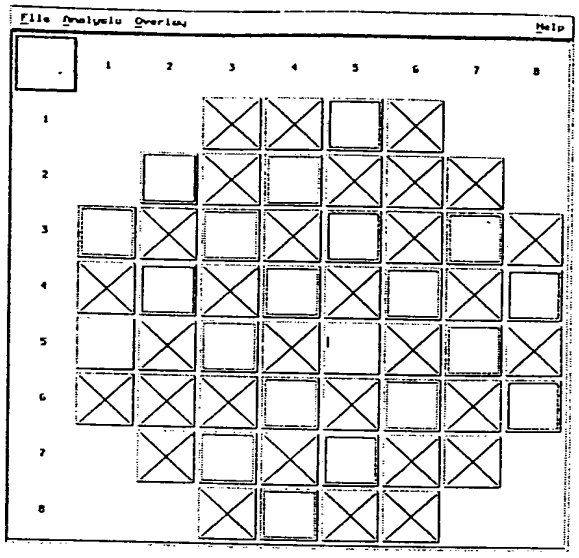

Figure 7: Wafer bitfail map of 524K ADMs found in Pattern SOI eDRAM hardware using the SC2 SIMOX blockout mask and 0.13 µm SOI process (screen test @ 9 ms retention). Outlined chips are screen-perfect ADMs.

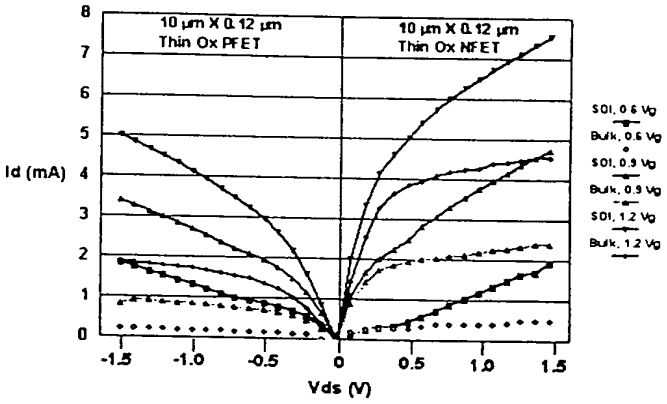

Figure 8: NFET and PFET Thin Oxide device characteristics on SOI and on bulk (10 X 0.12 µm; Vg =0.6 V, 0.9 V, 1.2 V).

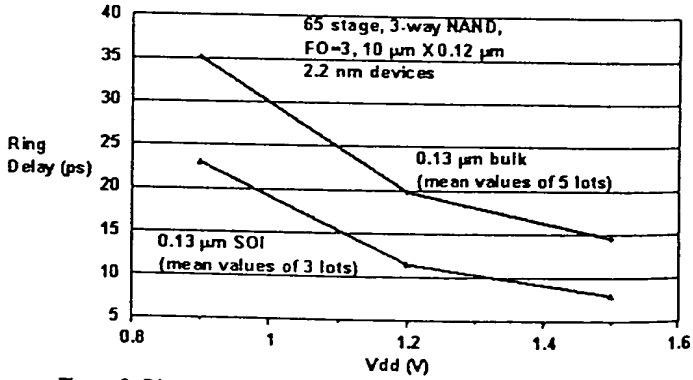

Figure 9: Ring oscillator delays found in 0.13 µm bulk eDRAM process and 0.13 µm SOI eDRAM process. Significant reductions in delays evident across all power supply voltages.